



c of c

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date January 17, 2007

Jennifer A. Steele
Jennifer A. Steele

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Brent Keeth

Attorney Docket No.: 500514.01

Patent No. : US 6,912,680 B1

Serial No. : 08/798,227

Issue Date : June 28, 2005

Filed : February 11, 1997

Title : MEMORY SYSTEM WITH DYNAMIC TIMING CORRECTION

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
JAN 24 2007
of Correction

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56),	[Omitted	--5,463,337 10/1995 Leonowich
References Cited,	references]	5,712,883 1/1998 Miller
U.S. Patent		5,764,092 6/1998 Wada et al.
Documents		6,125,157 9/2000 Donnelly--
Item (56),	"Ppaer 21.2,"	--Paper 21.2,--
References Cited,		
Other Publications,		
Chapman Reference		

JAN 25 2007

Item (56), References Cited, Other Publications, von Kaenel Reference	"Nov. 1996, pp .1715-1722."	--Nov. 1996, pp. 1715-1722.--
Column 1, Line 13	"must tightly controlled"	--must be tightly controlled--
Column 1, Line 25	"specified clock edge"	--specified clock edge,--
Column 1, Line 30	"propagation of delays."	--propagation delays.--
Column 2, Line 7	"versions of the maser clock"	--versions of the master clock--
Column 3, Line 13	"with edges the"	--with edges of the--
Column 4, Line 30	"and fine venires 96"	--and fine verniers 96--
Column 5, Line 63	"timing in not excessive,"	--timing is not excessive,--
Column 6, Line 4	"the new course"	--the new coarse--
Column 6, Line 40	"output timing:"	--output timing comprises:--
Column 7, Line 15	"time delay adjusting"	--time delay comprises adjusting--
Column 7, Line 45	"comparator:"	--comparator comprises:--
Column 7, Line 49	"a plurality of phase comparator,"	--a plurality of phase comparators,--
Column 8, Line 19	"a plurality of phase comparator,"	--a plurality of phase comparators,--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

JAN 25 2007

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Jan. 16, 2007

By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

H:\IP\Clients\Micron Technology\500\500514.01\500514.01 req cert correct.doc

JAN 25 2007



PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date January 17, 2007

Jennifer A. Steele
Jennifer A. Steele

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Brent Keeth

Attorney Docket No.: 500514.01

Patent No. : US 6,912,680 B1

Serial No. : 08/798,227

Issue Date : June 28, 2005

Filed : February 11, 1997

Title : MEMORY SYSTEM WITH DYNAMIC TIMING CORRECTION

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56),	[Omitted	--5,463,337 10/1995 Leonowich
References Cited,	references]	5,712,883 1/1998 Miller
U.S. Patent		5,764,092 6/1998 Wada et al.
Documents		6,125,157 9/2000 Donnelly--
Item (56),	"Ppaer 21.2,"	--Paper 21.2,--
References Cited,		
Other Publications,		
Chapman Reference		

JAN 25 2007

Item (56), References Cited, Other Publications, von Kaenel Reference	"Nov. 1996, pp .1715-1722."	--Nov. 1996, pp. 1715-1722.--
Column 1, Line 13	"must tightly controlled"	--must be tightly controlled--
Column 1, Line 25	"specified clock edge"	--specified clock edge,--
Column 1, Line 30	"propagation of delays."	--propagation delays.--
Column 2, Line 7	"versions of the maser clock"	--versions of the master clock--
Column 3, Line 13	"with edges the"	--with edges of the--
Column 4, Line 30	"and fine venires 96"	--and fine verniers 96--
Column 5, Line 63	"timing in not excessive,"	--timing is not excessive,--
Column 6, Line 4	"the new course"	--the new coarse--
Column 6, Line 40	"output timing:"	--output timing comprises:--
Column 7, Line 15	"time delay adjusting"	--time delay comprises adjusting--
Column 7, Line 45	"comparator:"	--comparator comprises:--
Column 7, Line 49	"a plurality of phase comparator,"	--a plurality of phase comparators,--
Column 8, Line 19	"a plurality of phase comparator,"	--a plurality of phase comparators,--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

JAN 25 2007

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Jan. 16, 2007

By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

H:\IP\Clients\Micron Technology\500\500514.01\500514.01 req cert correct.doc

JAN 25 2007

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : US 6,912,680 B1
DATED : June 28, 2005
INVENTOR(S) : Brent Keeth

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, U.S. Patent Documents	[Omitted references]	--5,463,337 10/1995 Leonowich 5,712,883 1/1998 Miller 5,764,092 6/1998 Wada et al. 6,125,157 9/2000 Donnelly--
Item (56), References Cited, Other Publications, Chapman Reference	"Ppaer 21.2,"	--Paper 21.2,--
Item (56), References Cited, Other Publications, von Kaenel Reference	"Nov. 1996, pp .1715- 1722."	--Nov. 1996, pp. 1715- 1722.--
Column 1, Line 13	"must tightly controlled"	--must be tightly controlled--
Column 1, Line 25	"specified clock edge"	--specified clock edge,--
Item (56), References Cited, U.S. Patent Documents	[Omitted references]	--5,463,337 10/1995 Leonowich 5,712,883 1/1998 Miller 5,764,092 6/1998 Wada et al. 6,125,157 9/2000 Donnelly--
Column 1, Line 30	"propogation of delays."	--propogation delays.--
Column 2, Line 7	"versions of the maser	--versions of the master

JAN 25 2007

	clock”	clock--
Column 3, Line 13	“with edges the”	--with edges of the--
Column 4, Line 30	“and fine venires 96”	--and fine verniers 96--
Column 5, Line 63	“timing in not excessive,”	--timing is not excessive,-
		-
Column 6, Line 4	“the new course”	--the new coarse--
Column 6, Line 40	“output timing:”	--output timing
		comprises:--
Column 7, Line 15	“time delay adjusting”	--time delay comprises
		adjusting--
Column 7, Line 45	“comparator:”	--comparator comprises:--
Column 7, Line 49	“a plurality of phase	--a plurality of phase
	comparator,”	comparators,--
Column 8, Line 19	“a plurality of phase	--a plurality of phase
	comparator,”	comparators,--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. 6,912,680 B1

No. add'l. copies
@ .30 per page



FORM PTO-1050 (REV. 3-82)

H:\IP\Clients\Micron Technology\500\500514.01\500514.01 PTO 1050.doc

2 5 2007

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : US 6,912,680 B1
DATED : June 28, 2005
INVENTOR(S) : Brent Keeth

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, U.S. Patent Documents	[Omitted references]	--5,463,337 10/1995 Leonowich 5,712,883 1/1998 Miller 5,764,092 6/1998 Wada et al. 6,125,157 9/2000 Donnelly--
Item (56), References Cited, Other Publications, Chapman Reference	"Ppaer 21.2,"	--Paper 21.2,--
Item (56), References Cited, Other Publications, von Kaenel Reference	"Nov. 1996, pp .1715- 1722."	--Nov. 1996, pp. 1715- 1722.--
Column 1, Line 13	"must tightly controlled"	--must be tightly controlled--
Column 1, Line 25	"specified clock edge"	--specified clock edge,--
Item (56), References Cited, U.S. Patent Documents	[Omitted references]	--5,463,337 10/1995 Leonowich 5,712,883 1/1998 Miller 5,764,092 6/1998 Wada et al. 6,125,157 9/2000 Donnelly--
Column 1, Line 30	"propogation of delays."	--propogation delays.--
Column 2, Line 7	"versions of the maser	--versions of the master

JAN 25 2007

	clock”	clock--
Column 3, Line 13	“with edges the”	--with edges of the--
Column 4, Line 30	“and fine venires 96”	--and fine verniers 96--
Column 5, Line 63	“timing in not excessive,”	--timing is not excessive,- -
Column 6, Line 4	“the new course”	--the new coarse--
Column 6, Line 40	“output timing:”	--output timing comprises:--
Column 7, Line 15	“time delay adjusting”	--time delay comprises adjusting--
Column 7, Line 45	“comparator:”	--comparator comprises:--
Column 7, Line 49	“a plurality of phase comparator,”	--a plurality of phase comparators,--
Column 8, Line 19	“a plurality of phase comparator,”	--a plurality of phase comparators,--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. 6,912,680 B1

No. add'l. copies

@ .30 per page

➔ _____

FORM PTO-1050 (REV. 3-82)

H:\IP\Clients\Micron Technology\500\500514.01\500514.01 PTO 1050.doc

JAN 25 2007